Description

EMBEDDED EEPROM CELL AND METHOD OF FORMING THE SAME

This application is a CON of 09/390,032 09/3/1999 PAT 6,432,067 which is a DIV of 08/961,972 10/31/1997 PAT 6,007,499.

Technical Field

The present invention relates generally to the non-volatile memory devices and more particularly to a non-volatile memory embedded logic device.

Background Art

Non-volatile memory cells such as EEPROM cells typically have a double-layer polycrystalline silicon ("poly") structure that includes a control gate layer and a floating gate layer. In contrast, semiconductor logic gates, having a control gate only, require only a single polysilicon process to form the control gate layer. To improve computing speed and reduce device size, non-volatile memory cells are sometimes embedded into logic chips. Since processes for forming a non-volatile memory cell and a logic gate are quite different, they are traditionally formed in a separate series of steps.

To reduce a total number of processing steps for a non-volatile memory embedded logic circuit, it is often desirable to form the embedded non-volatile memory cells using a single-layer poly structure. Figure 1A shows a cross-section of a typical single-layered EEPROM cell 10 dissected along a wordline. Figure 1B shows a cross-section of the same EEPROM cell 10 dissected along a bitline. With reference to Figure 1A, a P-channel single poly EEPROM cell 10 is formed in an N-well 14 provided within a P-substrate. With reference to Figure 1B, the EEPROM cell 10 includes a P-channel select transistor 24 and a P channel storage transistor 26. A first P+ diffusion region 28 serves as both a drain for storage transistor 26 and a source for select transistor